

Abstract

Methods and apparatus are disclosed herein for providing tri-state noise immunity for memory systems such as DDR memory systems, wherein

5        1) there are large variations in read data loop delay, and 2) strobe buses have similar termination and threshold voltages. In one embodiment, strobe receiver circuitry includes a counter and counter control logic. The counter updates a count in response to strobe edges of received strobe signals. The counter control logic enables the counter before each strobe signal is

10      received by generating control signals asynchronously with respect to the received strobe signals. The counter control logic also resets the counter after each strobe signal is received by receiving feedback from the counter and, in response to the feedback, resetting the counter asynchronously with respect to the received strobe signals. The strobe receiver circuitry may

15      form part of a DDR memory controller.

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